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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/343,872	Applicant(s) DAO ET AL.
	Examiner Kim T. Huynh	Art Unit 2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim R jections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Garnett et al. (US Patent 6,141,718)

Garnett discloses a high-bandwidth bus which comprises:

- a plurality of local busses (fig.2, 22, 24, 26) each for transferring data between a processing device (fig.2, 14, 16) and an associated memory module (DMA, 133); (col.15, lines 7-24), (col.6, lines 45-65)
- a cross-bus (fig.6, 80) means for transferring data among the plurality of local bus means, wherein said cross-bus means is coupled to each of the plurality of local busses by a bridge (fig.1, 12) means; (col.6, lines 45-65), (col.10, lines 23-36)
- a memory controller means for setting said bridge means to provide processing devices with access to memory modules, wherein controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules. (col.6, lines 45-

67), (col.9, lines 36-51), (col.16, lines 32-67), (col.15, lines 7-24), wherein Routing matrix is mapping to different paths, the storage (memory) control access to bridge and bridge controller responsive to control signals, data and addresses on the paths to the devices and arbiter selecting priority first come first serve)

- wherein the local busses each include two unidirectional (fig.6, 92, 94, 96) bit lines for each data bit and at least the cross-bus includes two unidirectional bit lines for each data bit, (wherein, multiplexer, (fig.9, 143), logically mapping for routing for each outgoing bit line that selects (col.6, lines 45-65), (col.10, lines 23-36), (fig.6, 94, 96, 92, the paths of data lines , wherein data routing via these paths from source to devices enhance unidirectional bit lines)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett et al. (US Patent 6,141,718)

a. As per claim 1, Garnett discloses a data transfer apparatus that comprises:

- a plurality of busses (fig.1, ie. 24, 26, D-bus) each configured to couple a processing device (fig.1, ie. 14, 16) to a corresponding memory module;(col.1, lines 52-65), (col.5, lines 18-54)
- at least one cross-bus (fig.6, 80) coupled to each of the plurality of busses by one or more bus bridges, wherein the bus bridge (fig.14, 12) each include a multiplexer (fig.9, 143) that are configurable to steer signals from the bus to the cross-bus, and are further configurable to steer signals from the cross-bus to the bus; (col.6, lines 45-65), (col.10, lines 23-36)
- a memory management unit configured to receive memory access requests from a plurality of processing devices and to responsively configured the bus bridges to steer address and data signals accordingly. (col.9, lines 36-51),
- wherein the plurality of busses includes two unidirectional (fig.6, 92, 94, 96) bit lines for each data bit and at least one cross-bus includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer (fig.9, 143) for each outgoing bit line that selects from three other incoming bit lines. (col.6, lines 45-65), (col.10, lines 23-36), (fig.6, 94, 96, 92), paths of data lines , wherein data routing via these paths from source to devices enhance unidirectional bit lines)

Garnett discloses all the limitations as above except a set of multiplexers It would have been obvious to one having ordinary skill in the art at the time the invention was made to include multiple of multiplexers,

since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

b. As per claim 11, Garnett discloses a method for transferring data between a set of memory modules and a set of processor units, wherein the method comprises:

- said processing units (fig.2, 14, 16) providing transfer requests to a memory manager; (col.15, lines 7-36), wherein processor set address from which to read and transfer, DMA emulates a device bus sending identical DMA requests)
- said memory manager setting a router(fig.6, 80) in a conflict-free access pattern in response to said transfer requests, wherein setting said router includes: (col.16, lines 32-40)
- said memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses; and ;(col.1, lines 52-65), (col.5, lines 18-54),
- wherein the plurality of busses includes two unidirectional (fig.6, 92, 94, 96) bit lines for each data bit and at least one cross-bus includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer (fig.9, 143) for each outgoing bit line that selects from three other incoming bit lines. (col.6, lines 45-65), (col.10, lines 23-36), (fig.6, 94, 96, 92), paths of data lines , wherein data

routing via these paths from source to devices enhance unidirectional bit lines)

- said processing units accessing memory modules via said router. ;(col.1, lines 52-65), (col.5, lines 18-54)

c. As per claims 2, 13, Garnett discloses the memory management unit includes a DMA controller coupled to the cross-bus and configurable to transfer a data between said memory modules. (col.9, lines 32-51), (col.6, lines 9-15); however Garnett fails to disclose controller configurable to transfer a block of data.

Although Garnett fails to disclose controller configurable for transferring a block data. However Garnett does teach configurable for routing data between processing devices but not explicitly the type of data for transferring. (col.6, lines 9-15).

Examiner takes Official Notice that a block of data type are well known in the art for data transferring between units. It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate the configuration for transferring a block data into Garnett's method so as for a greater flexibility for different type of data transferring and so as to be compatible with different type of systems.

d. As per claim 3, Garnett discloses the memory management unit includes an interrupt controller (fig.8, 134) configurable to assert an interrupt signal to said processing devices after completing transfer data. (col.16, lines 32-67), (col.17,

lines 1-26) wherein busy condition implies not allowing data transfer until complete)

e. As per claims 4,5, 6, 14, Garnett discloses the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to data transfers. (col.10, lines 23-61), wherein signals are held in buffer (fig.9, 149) implies queue, ready to be selected for transferring)

However Garnett fails to disclose single word of data, block data or message transfer.

Although Garnett fails to disclose controller configurable for transferring a single data word, block data, message transfer. However Garnett does teach configurable for routing data between processing devices but not explicitly the type of data for transferring. (col.6, lines 9-15).

Examiner takes Official Notice that block data or single data type, message transfer are well known in the art for transferring between units. It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate the configuration for transferring a block data or a single word of data or message transfer into Garnett's method so as for a greater flexibility for different type of data transferring and so as for compatible with different type of systems.

f. As per claim 7, Garnett discloses the memory management unit includes an interrupt controller (fig.8, 134) configurable to assert an interrupt signal to a

processing device that is an addressee of a data transfer request. (col.9, lines 36-55)

g. As per claim 8, Garnett discloses data transfer apparatus further comprising port logic (fig.6, 88) connected to the plurality of busses and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory. (col.2, lines 19-29) , (col.13, lines 10-13)

h. As per claim 10, plurality of busses includes at least three busses. (fig.6, 22, 24, 26), (col.4, lines 21-25)

i. As per claim 12, Garnett discloses wherein before setting said router(fig.6, 80), said memory manager determines said conflict-free access pattern in accordance with assigned priorities for each transfer request. (col.16, lines 32-67, setting priority first come first serve implies conflict-free)

Response to Amendment

5. Applicant's arguments with respect to claims 1-8, 10-15 have been considered but are deemed to be moot in view of the new grounds of rejection.

Conclusion

6. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.*

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

April 1, 2003

RUPAL DHARIA
PRIMARY EXAMINER